Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.075”**

**.040”**

**9 10 11 12**

**2 1 20 19**

**3**

**4**

**5**

**6**

**7**

**8**

**18**

**17**

**16**

**15**

**14**

**13**

**MASK**

**REF**

**244**

**PAD FUNCTION:**

1. **N. 1G**
2. **1A1**
3. **2Y4**
4. **1A2**
5. **2Y3**
6. **1A3**
7. **2Y2**
8. **1A4**
9. **2Y1**
10. **GND**
11. **2A1**
12. **1Y4**
13. **2A2**
14. **1Y3**
15. **2A3**
16. **1Y2**
17. **2A4**
18. **1Y1**
19. **N. 2G**
20. **VCC**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential: GND or FLOAT**

**Mask Ref: 244**

**APPROVED BY: DK DIE SIZE .040” X .075” DATE: 9/2/21**

**MFG: ZYTREX THICKNESS .021” P/N: 54LS244**

**DG 10.1.2**

#### Rev B, 7/1